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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,953	08/26/2003	Sean S. Kang	LAM1P177/P1139	4068

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/648,953	KANG ET AL.
	Examiner	Art Unit
	Julio J. Maldonado	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,14-17 and 21-39* is/are pending in the application.

4a) Of the above claim(s) *26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12,14-17,21-25,27,29,30,32,33,35 and 36* is/are rejected.

7)☒ Claim(s) *28,31,34 and 37-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection as set forth in Office Action mailed on 10/05/2004 is withdrawn in view of Applicants' response in view of the Ahn reference.

2. The cancellation of claims 2, 13, and 18-20, and the addition of claims 21-39 as set forth in Paper filed on 01/05/2005 is acknowledged.

3. Claims 1, 3-12, 14-17, and 21-39 are pending in the present application.

Claim Objections

4. Claims 28, 31, 34 and 37 are objected to because of the following informalities: claims 31 recite"...wherein the depositing the conformal layer provides no layer deposited on a bottom of a photoresist (or mask as in claim 28) feature.". However, according to Fig.3B, there is no photoresist at the bottom of the hole 314, where conformal layer 320 is deposited. It is suggested to change claims 31, 34 and 37 to recite --wherein the depositing the conformal layer provides a portion of the bottom of the via without deposited conformal layer--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-6, 9-12, 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Kinoshita et al. (U.S. 6,780,708 B1) and Kim et al. (U.S. 6,656,282).

Chung et al. (Figs.1-3B) teach a method of patterning a metal layer (110) deposited on a substrate (100) comprising providing said substrate (100); depositing said metal layer (110); forming a photoresist layer; patterning said photoresist layer to form a photoresist patterns (130), wherein said photoresist patterns (130) include vertical sidewalls with a first critical dimension; depositing a conformal layer (150) on the sidewalls of said photoresist patterns and on the surface of said metal layer (110); anisotropically etching said conformal layer (150) to form conformal layer spacers on the sidewalls of said photoresist patterns (130), reducing the space between said photoresist patterns (130); and etching said metal layer (110) underlying said photoresist patterns (130) and conformal layer spacers forming metal patterns, wherein the space between said metal patterns is lower than said space between said photoresist patterns and wherein the conformal layer has substantially the same sidewall thickness from atop to a bottom of the feature (column 2, line 54 – column 4, line 34).

Since the same materials are treated the same way, it is inherent from the teachings of Chung et al. that the photoresist patterns of Chung et al. have a first critical dimension, and that the addition of conformal layer spacers reduce the critical dimension of said photoresist patterns, resulting in metal patterns with a second critical dimension, which is less than a first critical dimension, thus arriving at the same result of the claimed invention.

Furthermore, Chung et al. teach wherein said conformal layer is made from organic or inorganic materials using plasma enhanced chemical vapor deposition

(PECVD) or low pressure chemical vapor deposition (LPCVD) (Chung et al. column 3, lines 21 – 26), but fail to teach wherein depositing said material comprises a first deposition with a first gas chemistry to form a first deposition plasma; and a second deposition with a second gas chemistry to form a second deposition plasma, wherein the first gas chemistry is different than the second gas chemistry. However, Kinoshita et al. (Figs.1-6) in a related method to form metal pattern teach the steps of forming a metal layer (18) on a substrate (12); forming a mask layer (34a) on the metal layer (18); and forming a conformal layer spacer (46d) on the sidewalls of said mask layer (34a), wherein said conformal layer spacer (46d) is made from a material selected from the group including silicon oxide, silicon nitride and other nitrides. Furthermore, Kinoshita et al. teach silicon oxide layers and silicon nitride layers can be deposited using processes selected form the group including PECVD and atomic layer deposition (ALD) (column 8, line 44 – column 10, line 15).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chung et al. and Kinoshita et al. to enable forming the conformal layer of Chung et al. according to the teachings of Kinoshita et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the conformal layer of Chung et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Chung et al. and Kinoshita et al. fail to teach using a plasma deposition method to deposit said silicon nitride layer. However, Kim et al.

teach a method of depositing silicon nitride including using plasma ALD to deposit said nitride layer (column 1, line 27 – column 2, line 14 and column 6, lines 45 – 67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references of Chung et al. and Kinoshita with Kim et al. to enable depositing the silicon nitride layer of Chung and Kinoshita according to the teachings of Kim et al. because this would result in a low temperature deposition process with reduced impurities (column 2, lines 8 – 14).

Still, the combined teachings of Chung et al., Kinoshita et al. and Ahn et al. substantially teach all aspects of the invention but fail to disclose wherein the second critical dimension is not greater than 60% of first critical dimension, wherein the conformal layer has a sidewall thickness and a photoresist feature bottom thickness, wherein the sidewall thickness is greater than the photoresist feature bottom thickness, and wherein the photoresist layer is formed from 248 nm photoresist and the feature has a CD not greater than 140 nm. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d

459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Kinoshita et al. (U.S. 6,780,708 B1) and Kim et al. (U.S. 6,656,282) as applied to claims 1, 3-6, 9-12, 14-17 above, and further in view of Yamamoto et al. (U.S. 4,151,034).

The combined teachings of Chung et al., Kinoshita et al. and Kim et al. substantially teach all aspects of the invention but fail to disclose stripping the photoresist mask and deposited conformal layer with a single stripping step, wherein said striping comprises ashing the photoresist mask and the deposited layer. However, Yamamoto et al. teach a method of simultaneously etch a photoresist layer and a silicon nitride layer using ashing (column 1, lines 7 – 17). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chung et al., Kinoshita et al. and Kim et al. with the teachings of Yamamoto to enable the etching step of Chung et al., Kinoshita et al. and Kim et al. to be performed according to the teachings of Yamamoto et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Chung et al., Kinoshita et al. and Kim et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07.), and furthermore, because this etching

technique provide easier operation, higher reliability and no environmental pollution compared to conventional etching processes (Yamamoto et al., column 1, lines 7 – 17).

8. Claims 21-24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Moslehi (U.S. 5,273,609).

In reference to claims 21 and 35, Chung et al. (Figs.1-3B) teach a method of patterning a metal layer (110) deposited on a substrate (100) comprising providing said substrate (100); depositing said metal layer (110); forming a photoresist layer; patterning said photoresist layer to form a photoresist patterns (130), wherein said photoresist patterns (130) include vertical sidewalls with a first critical dimension; depositing a conformal layer (150) on the sidewalls of said photoresist patterns and on the surface of said metal layer (110); anisotropically etching said conformal layer (150) to form conformal layer spacers on the sidewalls of said photoresist patterns (130), reducing the space between said photoresist patterns (130); and etching said metal layer (110) underlying said photoresist patterns (130) and conformal layer spacers forming metal patterns, wherein the space between said metal patterns is lower than said space between said photoresist patterns and wherein the conformal layer has substantially the same sidewall thickness from atop to a bottom of the feature (column 2, line 54 – column 4, line 34).

Since the same materials are treated the same way, it is inherent from the teachings of Chung et al. that the photoresist patterns of Chung et al. have a first critical dimension, and that the addition of conformal layer spacers reduce the critical dimension of said photoresist patterns, resulting in metal patterns with a second critical

dimension, which is less than a first critical dimension, thus arriving at the same result of the claimed invention.

Furthermore, Chung et al. teach wherein said conformal layer is made from organic or inorganic materials using plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD) (Chung et al. column 3, lines 21 – 26), but fail to teach wherein said deposition and said etching in the same chamber. However, Moslehi (Fig.1) teaches a method of plasma depositing and etching materials used to produce a semiconductor device, wherein said depositing and said etching are performing in the same chamber (column 7, lines 39 –64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chung et al. and Moslehi to enable performing the etching and the depositing of Chung et al. in the reaction chamber of Moslehi for the further advantage of reducing thermal stresses on the semiconductor device and eliminate gas flow transient and stabilization times (column 6, lines 36 – 41).

In reference to claim 22-24, the combined teachings of Chung et al. and Moslehi substantially teach all aspects of the invention but fail to disclose wherein a ratio of the widths of the mask lines to the widths of the mask spaces is less than 1:1 and wherein a ratio of the widths of the conductive lines to the widths of the spaces between the conductive lines is not less than 1:1 or greater than 1:1; and wherein the width of the mask spaces is more than 50% greater than the widths of the spaces between the conductive lines. However, the selection of the above-mentioned width spaces is obvious because it is a matter of determining optimum process condition by routine

experimentation with a limited number of species to obtain a desired pattern. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above-mentioned ratios to arrive at the claimed invention.

9. Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (U.S. 5,296,410) in view of Moslehi (U.S. 5,273,609).

In reference to claim 21, Yang (Figs.4-7) teaches an etching method including the steps of placing a conductive layer (20) on a substrate (10); forming a mask, wherein the mask defines a plurality of mask lines (30) with mask spaces between the mask lines (30), wherein the mask spaces have a width and wherein the mask lines (30) have a width and have sidewalls; depositing a conformal layer (50) over the sidewalls of the mask lines (30); etching the conductive layer (20) through the mask lines (30) to form conductive lines (40) and spacers (50a) between the conductive lines (40), wherein the conductive lines (40) have a width and the spaces between the conductive lines (40) have widths, wherein the widths of the spaces between the conductive lines (40) is less than the widths of the mask line spaces, and wherein the widths of the conductive lines (40) is greater than the widths of the line masks (30) (column 3, line 54 – column 4, line 55).

Yang fails to teach wherein said deposition and said etching in the same chamber. However, Moslehi (Fig.1) teaches a method of plasma depositing and etching materials used to produce a semiconductor device, wherein said depositing and said etching are performing in the same chamber (column 7, lines 39 –64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to combine the teachings of Yang and Moslehi to enable performing the etching and the depositing of Yang in the reaction chamber of Moslehi for the further advantage of reducing thermal stresses on the semiconductor device and eliminate gas flow transient and stabilization times (column 6, lines 36 – 41).

In reference to claim 25, the combined teachings of Yang and Moslehi teach etching the conformal layer and the conductive layer, sequentially, wherein in the etching process, the conformal layer and the conductive layer have an etching selectivity of about 10 to 1, for stable pattern formation (Yang, column 4, lines 24 – 36). Also, the combination of Yang and Moslehi also disclose that the etching recipe to etch the conformal layer is different than that of the conductive layer because of the etching selectivity.

10. Claims 27 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Moslehi (U.S. 5,273,609) as applied to claims 21-24 and 35 above, and further in view of Yamamoto et al. (U.S. 4,151,034).

The combined teachings of Chung et al. and Moslehi substantially teach all aspects of the invention but fail to disclose stripping the photoresist mask and deposited conformal layer with a single stripping step, wherein said striping comprises ashing the photoresist mask and the deposited layer in the same chamber.

However, Yamamoto et al. teach a method of simultaneously etch a photoresist layer and a silicon nitride layer using ashing (column 1, lines 7 – 17). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chung et al. and Moslehi with the teachings of Yamamoto to enable the etching step

of Chung et al. and Moslehi to be performed according to the teachings of Yamamoto et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Chung et al. and Moslehi and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07.), and furthermore, because this etching technique provide easier operation, higher reliability and no environmental pollution compared to conventional etching processes (Yamamoto et al., column 1, lines 7 – 17).

11. Claims 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Kinoshita et al. (U.S. 6,780,708 B1) and Kim et al. (U.S. 6,656,282) as applied to claims 1, 3-6, 9-12, 14-17 above, and further in view of Moslehi (U.S. 5,273,609).

The combined teachings of Chung et al., Kinoshita et al. and Kim et al. substantially teach all aspects of the invention but fail to disclose wherein depositing the conformal layer and etching features are performed in the plasma processing chamber. However, Moslehi (Fig.1) teaches a method of plasma depositing and etching materials used to produce a semiconductor device, wherein said depositing and said etching are performing in the same chamber (column 7, lines 39 –64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chung et al., Kinoshita et al. and Kim et al. with Moslehi to enable performing the etching and the depositing of Chung et al., Kinoshita et al. and Kim et al. in the reaction chamber of Moslehi for the further advantage of reducing

thermal stresses on the semiconductor device and eliminate gas flow transient and stabilization times (column 6, lines 36 – 41).

12. Claims 30 and 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. 6,750,150 B2) in view of Kinoshita et al. (U.S. 6,780,708 B1), Kim et al. (U.S. 6,656,282) and Moslehi (U.S. 5,273,609) as applied to claims 1, 3-6, 9-12, 14-17, 29 and 33 above, and further in view of Yamamoto et al. (U.S. 4,151,034).

The combined teachings of Chung et al., Kinoshita et al., Kim et al. and Moslehi substantially teach all aspects of the invention but fail to disclose stripping the photoresist mask and deposited conformal layer with a single stripping step, wherein said striping comprises ashing the photoresist mask and the deposited layer in the same chamber. However, Yamamoto et al. teach a method of simultaneously etch a photoresist layer and a silicon nitride layer using ashing (column 1, lines 7 – 17). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chung et al., Kinoshita et al., Kim et al. and Moslehi with the teachings of Yamamoto to enable the etching step of Chung et al., Kinoshita et al., Kim et al. and Moslehi to be performed according to the teachings of Yamamoto et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Chung et al., Kinoshita et al., Kim et al. and Moslehi and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07.), and furthermore, because this etching technique provide easier operation, higher

reliability and no environmental pollution compared to conventional etching processes (Yamamoto et al., column 1, lines 7 – 17).

Allowable Subject Matter

13. Claims 28, 31, 34 and 37 would be allowable if rewritten to overcome the claim objections as set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. Claims 38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach wherein the first deposition is selected from the group of the group a bread loafing deposition and a faceting deposition and the second deposition is selected from the group of the group of a bread loafing deposition and a faceting deposition , the first deposition and second deposition are not both bread loafing depositions and are not both faceting depositions as recited in claims 38 and 39.

Response to Arguments

16. Applicant's arguments with respect to claims 1, 3-12, 14-17, and 21-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
March 14, 2005

George Fourson
Primary Examiner